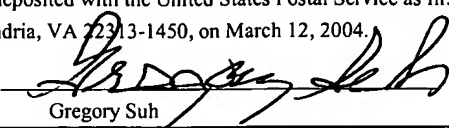




PATENT
Docket No. SPLX.P0100

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Gregory Suh

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Steven Teig, et al.

Serial No.: 10/062,993

Filing Date: 1/31/02

For: METHOD AND APPARATUS FOR
PERFORMING TECHNOLOGY
MAPPING

**INFORMATION DISCLOSURE
STATEMENT UNDER 37 C.F.R. § 1.97**

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Dear Sir:

Pursuant to 37 C.F.R. § 1.97 and § 1.98, applicants submit with this Information Disclosure Statement the attached Form PTO-1449, and copies of the documents listed in the 1449 form for consideration by the Examiner. The Examiner is requested to make these documents of record. Applicants would appreciate the Examiner initialing and returning the Form PTO-1449, indicating that the information has been considered and made of record herein.

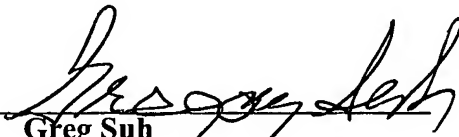
This Information Disclosure Statement under 37 C.F.R. § 1.97 is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

This Information Disclosure Statement is submitted concurrently with a Request for Continued Examination for the above-identified patent application, accordingly, no fee or separate requirements are required.

However, in the unlikely event that the Patent Office determines that additional fees, extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 50-1128** referencing SPLX.P0100. However, the Assistant Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

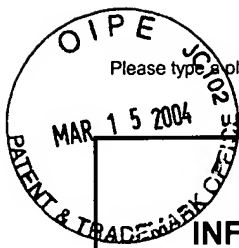
Dated: March 12, 2004

Respectfully submitted,

By: 
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				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
				Examiner Name	Kik, Phallaka
Sheet	1	of	1	Attorney Docket Number	SPLX.P0100

U.S. PATENT DOCUMENTS						
Examiner* Initials	Cite No. ¹	U.S. Patent Document		Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
	1.	5,521,835		05-28-1996	Trimberger	
	2.	5,610,829		03-11-1997	Trimberger	
	3.	6,035,107		03-07-2000	Kuehlman et al.	
	4.	6,216,252	B1	04-10-2001	Dangelo et al.	
	5.	6,334,205		12-25-2001	Iyer et al.	
	6.	6,470,478	B1	10-22-2002	Bargh et al.	
	7.	6,496,972	B1	12-17-2002	Segal	
	8.	6,523,156	B2	02-18-2003	Cirit	
	9.	6,574,779	B2	06-03-2003	Allen et al.	

NON PATENT LITERATURE DOCUMENTS					
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	10.	Yi, J. H. et al., Technology Mapping for Storage Elements Based on BDD matching, Proceedings of the 40 th Midwest Symposium on Circuits and Systems, pp. 1099-1102, vol.2, August 1997.			

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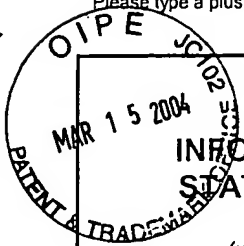
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				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2122
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Sheet	1	of	2	Attorney Docket Number	SPLX.P0100

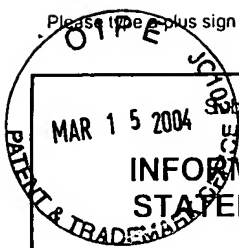
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		Serial Number				
	1.	10/062,017		Steven Teig & Asmus Hetzel	01-31-02	
	2.	10/061,459		Steven Teig & Asmuz Hetzel	01-31-02	
	3.	10/062,014		Steven Teig & Asmus Hetzel	01-31-02	
	4.	10/062,044		Steven Teig & Asmuz Hetzel	01-31-02	
	5.	10/066,264		Steven Teig & Asmus Hetzel	01-31-02	
	6.	10/066,188		Steven Teig & Asmus Hetzel	01-31-02	
	7.	10/062,992		Steven Teig & Asmuz Hetzel	01-31-02	
	8.	10/061,474		Steven Teig & Asmus Hetzel	01-31-02	
	9.	10/061,719		Steven Teig & Asmus Hetzel	01-31-02	
	10.	10/066,456		Steven Teig & Asmus Hetzel	01-31-02	
	11.	10/062,047		Steven Teig & Asmuz Hetzel	01-31-02	

U.S. PATENT DOCUMENTS						
Examiner* Initials	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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	12.	5,649,165		Jain et al.	07-15-97	
	13.	6,301,687	B1	Jain et al.	10-09-01	

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				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

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	14.	D. Jongeneel, R. Otten, Y. Watanabe and R. K. Brayton, Area and Search Space Control for Technology Mapping, 37 th Design Automation Conference, 86-91, 2000.	
	15.	Henrik Reif Andersen, An Introduction to Binary Decision Diagrams, October 1997 (minor revisions April 1998), 36 pp.	
	16.	Jerry Burch and David Long, Efficient Boolean Function Matching, Proc. ICCAD 1992, 408-411.	
	17.	John Fishburn, A Depth-Decreasing Heuristic for Combinational Logic; or How to Convert Ripple-Carry Adder into a Carry-Lookahead Adder or Anything In-Between, Proceedings of the 27 th Design Automation Conference, 361-364, 1990.	
	18.	Kamal Chaudhary and Massoud Pedram, A Near Optimal Algorithm for Technology Mapping Minimizing Area under Delay Constraints, Proceedings of the 29 th Design Automation Conference, 492-498, 1992.	
	19.	Kurt Keutzer, DAGON: Technology Binding and Local Optimization by DAG Matching, Proceedings of the 24 th Design Automation Conference, 341-347, 1987	
	20.	Randal Bryant, Symbolic Boolean Manipulation with Ordered Binary Decision Diagrams, CMU CS Tech Report CMU-CS-92-160.	
	21.	Uwe Hinsberger and Reiner Kolla, Boolean Matching for Large Libraries, Proceedings of the 35 th Design Automation Conference, 206-211, June 1998.	
	22.	Yuji Kukimoto, Robert K. Brayton, and Prashant Sawkar, Delay-Optimal Technology Mapping by DAG Covering, Dept. of Electrical Engineering and Computer Science, University of California, Berkeley, Strategic CAD Laboratories, Intel Corp., October 1997.	
	23.	Zbigniew J. Czech, et al., An Optimal Algorithm for Generating Minimal Perfect Hashing Functions, Information Processing Letters, 43(5): 257-264, October 1992	

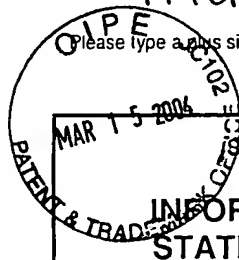
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				Examiner Name	
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U.S. PATENT DOCUMENTS

Examiner* Initials	Cite No. ¹	U.S. Patent Document Number	Kind Code ² (if known)	Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	5,519,630		05-21-1996	Nishiyama et al.	
	2.	5,537,341		07-16-1996	Rose et al.	
	3.	5,696,974		12-09-1997	Agrawal et al.	
	4.	5,574,441		05-19-1998	Tokunoh et al.	
	5.	5,787,010		07-28-1998	Schaefer et al.	
	6.	6,023,566		02-08-2000	Belkhale et al.	
	7.	6,301,696	B1	11-09-2001	Lien et al.	

NON PATENT LITERATURE DOCUMENTS

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	8.	Crastes, M. et al., A Technology Mapping Method Based on Perfect and Semi-Perfect Matchings, Design Automation Conference, 1991, 28 th ACM/IEEE, June 17-21, 1991, pp. 93-98.	
	9.	Devadas, S. et al., Synthesis and Optimization for robustly delay-fault testable combinational logic circuits, Design Automation Conference, 1990, 27 th ACM/IEEE, June 24-28, 1990, pp. 221-227.	

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